FUNDAMENTALS OF SEMICONDUCTOR PROCESSING TECHNOLOGIES

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This process is also referred to as **lift-off.** For lift-off to occur, the thickness of the deposited film must be smaller than the resist thickness and a gap must remain between the two materials.

Very stringent requirements are imposed on etch processes. Image and sidewall slope control and pattern reproducibility must be achieved across the wafer, wafer to wafer, and run to run. While dry, plasma-assisted etching is best suited to meet the above requirements for submicron technologies, wet etch techniques are still used in some special applications where large tolerances in image dimensions are acceptable.

Definition of Terms

The film thickness removed per unit time is called the **etch rate.** The etchant must remove the selected material without appreciably affecting the properties of other materials on the surface. The ratio of the etch rate of the material to be removed to the etch rate of another material is called the etch **selectivity.** The most important characteristics of an etchant are the etch rate, selectivity, and dimensional control that can be achieved on the pattern to be etched.

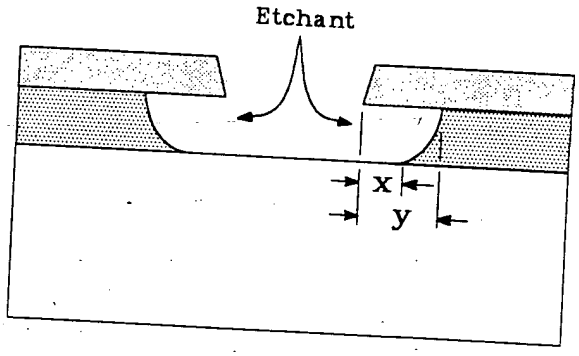

Fig. 5.7 Definition of two lateral etch dimensions, illustrated for isotropic etching. x is referred to etch bias and y as undercut.

When etching proceeds at the same rate in all directions, it is said to be **isotropic** (Fig. 5.7). When the etch rate is considerably larger in one direction than in another, etching is termed **anisotropic.** It is important to distinguish between lateral etching at the top and bottom interfaces of the etched layer when a mask

is used to pattern the film. The mask typically consists of a material that is not attacked by the etchant. The top dimension y is commonly referred to as **undercut.** It is approximately equal to the film thickness, until etching reaches the film-substrate boundary. Overetching beyond this point increases the undercut and radius of sidewall curvature. For a long overetch, the sidewalls become essentially vertical (Fig. 5.8). Overetching is necessary to ensure complete removal of the selected film because of nonuniformities in the wafer topography and variations in the film thickness and etch rate. The dimension x in Fig. 5.7 at the film-substrate interface is called **etch bias.**

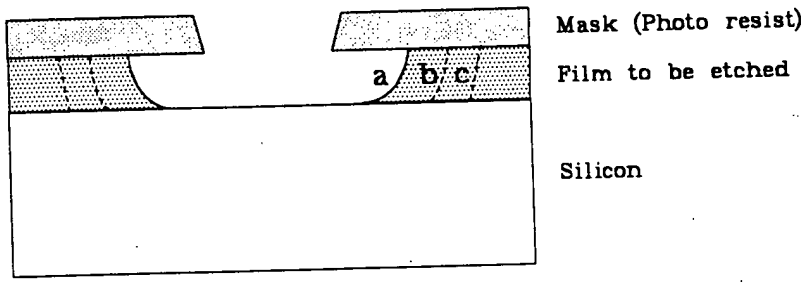

Fig. 5.8 Effect of isotropic overetching on undercutting and sidewall slope: (a) no overetch, (b) moderate overetch, (c) long overetch.

A comparison between isotropic, moderately anisotropic, and highly anisotropic etching is shown schematically in Fig. 5.9. Vertical anisotropic etching of a film that is deposited conformably in a groove or over a step leaves film "stringers" or "spacers" on the sidewalls, while isotropic etching removes the film entirely (Fig. 5.10).

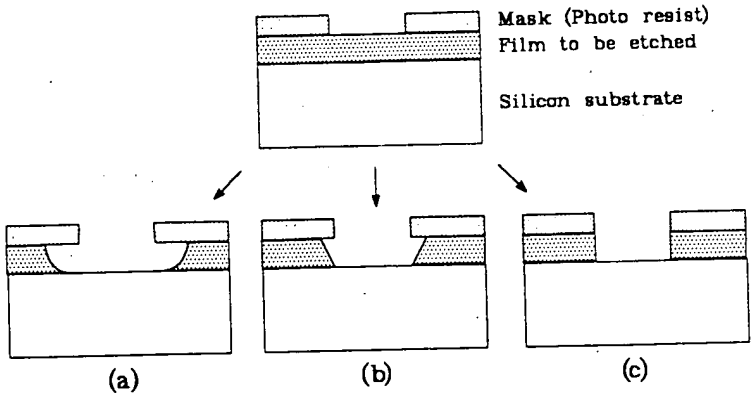

Fig. 5.9 Etch directionality. (a) Isotropic. (b) Moderately anisotropic (c) Strongly anisotropic (vertical).

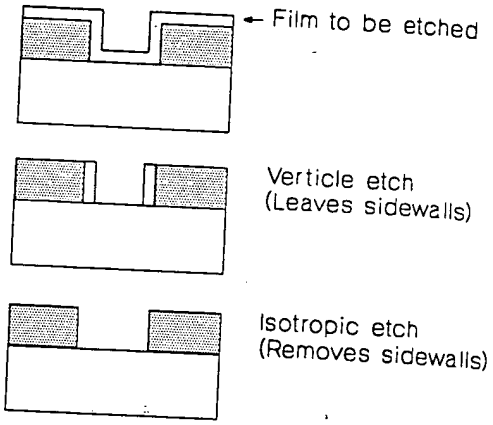

Fig. 5.10 Effect of etch directionality on sidewall film.
(a) Conformal film deposition over step.
(b) Anisotropic etching leaves sidewall almost intact.
(c) Sidewall fully removed by isotropic etching.

5.2.1 Wet Etching

Wet etching is performed by immersing the wafers in an appropriate solution (e.g., in batches of 25 wafers) or by spraying the wafer with the etchant solution.

The Silicon-Dioxide Etch

Selective removal of silicon-dioxide films from silicon surfaces is the most frequently repeated etching step in device processing. Etching of SiO_2 is typically achieved by immersing the wafer in a dilute solution of hydrofluoric acid (HF), buffered with ammonium fluoride (NH_4F). This is referred to as a buffered HF solution (BHF), also called Buffered-Oxide Etch (BOE). Buffering HF with NH_4F replenishes the fluoride ions as they are consumed, and results in well controlled etching without appreciably attacking photoresist. Since SiO_2 is an amorphous material, its etching in BHF is isotropic. The net reaction is [22]:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O\,.$$

H_2SiF_6 is a soluble complex which can be removed from the vicinity of the surface by stirring. Spray etching has gradually

replaced immersi
rate and uniformi
it also reduces lat

Table 5.2
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faster etch rate th

The prese
etch rate significa
oxide results in a
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attacks SiO_2, and
[23]. With about
nm/s in BHF, co
called P-etch is a
used used to selec
P-etch increases r
Similarly, the etch
arly with the B_2O_3

Table 5.2 Appro
25 °C[a]

Type of SiO_2
Dry grown
Wet grown
CVD deposited
Sputtered

a) 10 parts of 454
b) Annealed at app
c) Not annealed

The etch ra
be increased by in
oxide, causing stres
used to control th
gradually increasin

metric and the capacitive coupling between electrode and plasma is greater at the larger electrode; the plasma potential is closer to the potential of the larger electrode than to that of the smaller electrode. If the area of the powered electrode is significantly smaller than the grounded area, as is the case for typical planar reactors, the plasma potential is small, in the range ≃20 - 50 V above ground, and a larger sheath potential appears at the smaller electrode than at the large electrode [36]. The average sheath potential of the smaller electrode varies from about 0.25 to 0.5 of the peak to peak voltage of the applied RF signal as the reactor goes from a symmetric to a very asymmetric configuration [32]. In summary, for very asymmetric designs, a large sheath potential difference exists at the smaller electrode causing high-energy ion bombardment of a surface placed on the electrode. The mean voltages across the two sheaths are divided according to the relationship

$$\frac{V_1}{V_2} \simeq \left(\frac{A_2}{A_1}\right)^4, \qquad 5.5$$

where A_1 is the area of the small powered electrode, and A_2 the area of the large grounded electrode [37].

Physical Etch Processes

If a chemically inert gas, such as argon, is ionized and accelerated to impinge on a wafer surface, material can be removed from the surface by momentum transfer, a process similar to sandblasting. This process is used in three distinct modes. When the wafer is immersed in a plasma and subjected to bombardment with high-energy plasma ions which are accelerated across the sheath, the process is termed **sputter etching** [38,39]. When the wafer is physically separated from the plasma and a broad ion beam extracted from the plasma, collimated and accelerated to impinge on the wafer surface in a definite direction with respect to the feature to be etched, the process is called **ion-beam milling** [40 – 42]. The third mode is to spatially selective etch the material with a beam of ions (typically Ga^+), focused to submicron diameter (Chap. 3). This technique is referred to as **focused ion**

beam (FIB) etching or milling. Although FIB milling has not emerged for dry etching of silicon patterns, it has become an indispensable tool for restructuring a pattern on a mask or integrated circuit (unwanted opaque pattern milled-off), or for diagnostic cross-sectioning of microstructures [43].

Sputter etching and broad ion-beam milling use high-energy ($\geq$ 500 eV), inert gas ions (typically Ar^+) to dislodge material from the wafer surface - a highly anisotropic etch process. The principle of sputter etching is shown schematically in Fig. 5.17. The wafers are mounted on the powered electrode, immersed in a glow discharge at a pressure of 1-10 mTorr. Noble gas ions are created in the plasma and accelerated toward the wafer surface. The electric field profile and gas density around the electrode is such that most of the accelerated ions impinge on the wafer surface at normal incidence. If the ion energy is above a threshold value, atoms, molecules or ions are ejected from the wafer surface and vertical etch profiles can be achieved.

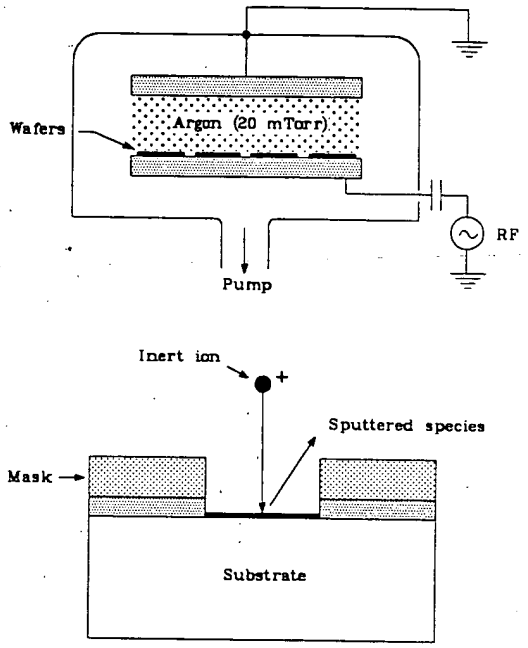

Fig. 5.17 Principle of sputter etching.

Physical-Chemical Etch Techniques

The reaction-rate between gas and wafer surface can be greatly increased by combining chemical and physical processes at or near the surface. Anisotropic etching can be achieved by impinging high-energy ions, electrons, or photons onto the surface, enhancing the reaction between the gas and horizontal surfaces with little attack on vertical sidewalls.

Reactive Ion Etching (RIE)

The most common etch technique in the manufacture of VLSI/ULSI silicon devices is the so-called reactive-ion etch (RIE) [50]. Positive plasma ions in a parallel-plate RF reactor are used to provide a source of energetic particle bombardment for the etched surface, producing vertical edges in the etched film with negligible undercutting (Fig. 5.20). Ion bombardment increases the reaction rate of spontaneously occurring processes and/or prompts reactions which do not occur without radiation.

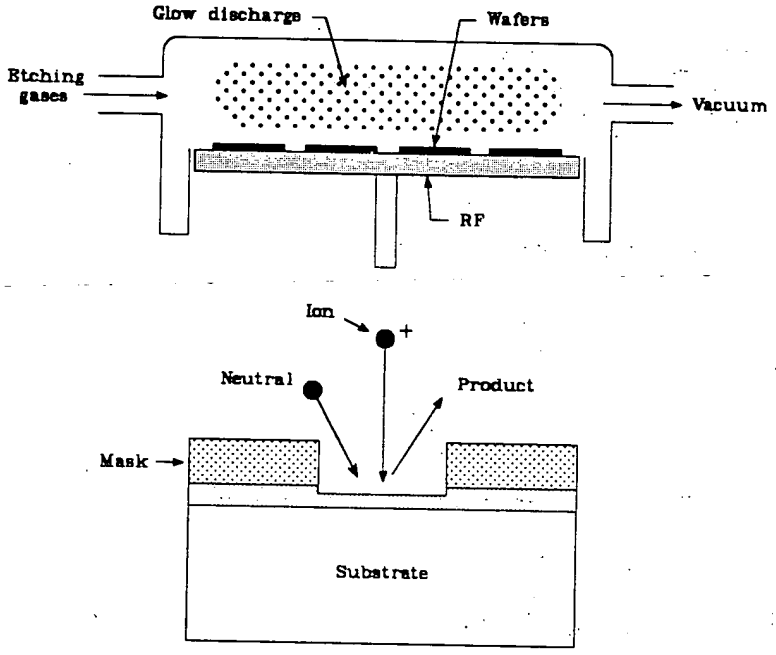

Fig. 5.20 Reactive-ion etch system. The wafers are placed on the powered electrode of a parallel-plate RF reactor. Horizontal surfaces are subjected to both reactant species and impinging ions, while vertical sidewalls are only subjected to reactive species.

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